FP101 Application Circuit for DCS Bands

Summary:

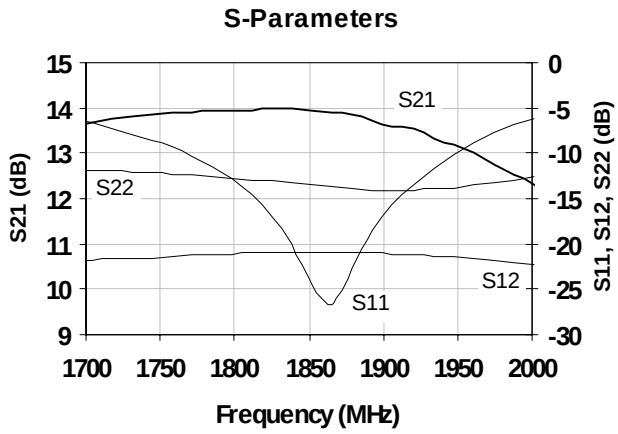
This application note details the operation and schematic of an application circuit using a WJ Communications **FP101** device optimized for the PCS bands. This circuit offers excellent performance for efficiency, IP3, P1dB, and noise figure using the WJ Communications low-cost FET between 1800 - 1900 MHz. This circuit is ideal for use as driver circuits for infrastructure equipment in PCS applications where cost and performance are critical parameters.

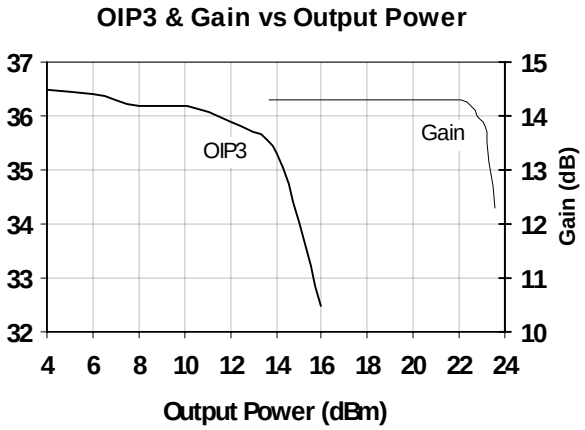
Frequency	1850 MHz
S21 - Gain	13.9 dB
S11 - Input Return Loss	-23.6 dB
S22 - Output Return Loss	-13.5 dB
S12 - Isolation	-20.9 dB
Output P1dB	23.3 dBm
Output IP3[1]	36.2 dBm
Noise Figure	3.6 dB
Drain Bias	5 V @ 100 mA

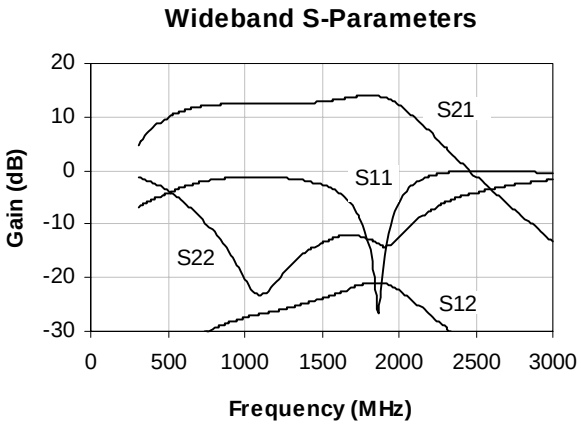
Details:

The drain voltage can be increased up +8 V for increased output power performance (higher P1dB). The gate voltage can be adjusted so that the drain bias can be anywhere between 50 - 150 mA, depending on the required performance using this device.

An optional temperature-compensation active-bias circuit is recommended for use with the application circuit, which requires two standard voltage (± 5 V) supplies. The circuit schematic, shown in Figure 2, uses dual PNP transistors to provide a constant drain current into the FET. Temperature compensation is achieved by tracking the voltage variation with the temperature of the emitter-to-base junction of the PNP transistors. Thus the transistor emitter voltage adjusts the voltage incident at the gate of the FET so that the device draws a constant current, regardless of the temperature. Two fixed voltage supplies are needed for operation. A Rohm dual transistor, UMT1N, and a dual chip resistor (8.2 kΩ) are recommended to minimize board space.







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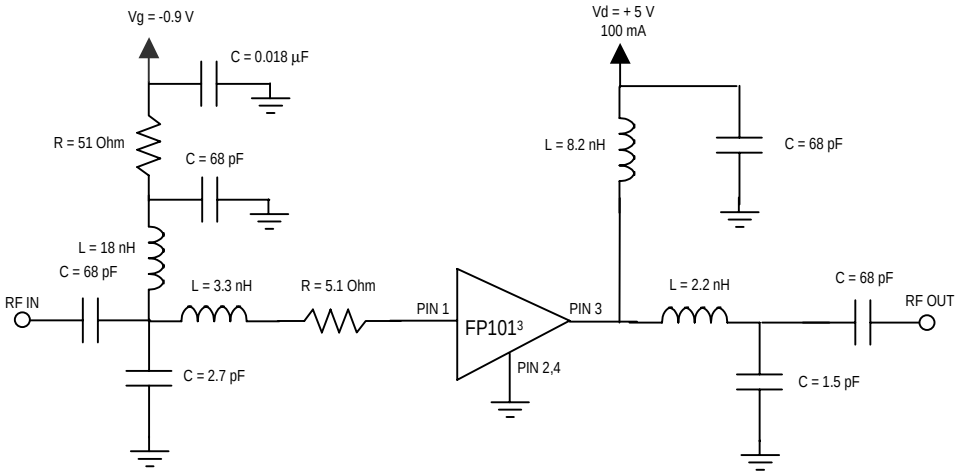

Figure 1. FP101 1800 – 1900 MHz Application Circuit Schematic[2]

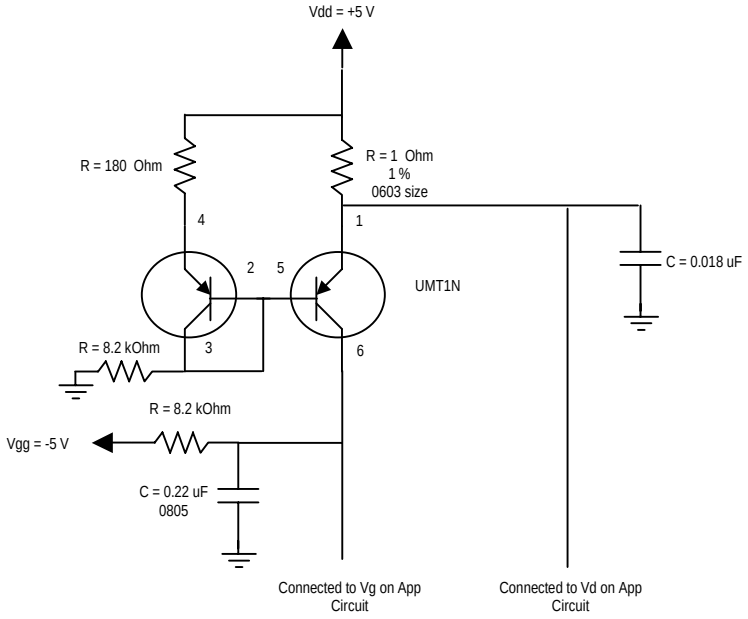

Figure 2. Optional Constant Current DC Bias Circuit Schematic

[1] OIP3 is measured with 2 tones at an output power of 10 dBm/tone with 10 MHz spacing at 1900 MHz. The suppression on the largest IM3 product is used to calculate OIP3 using a 2:1 slope rule. Test parameters were taken at 25 °C.

[2] All components are 0603 size. Toko LL1608-FH chip inductors and AVX ±0.1 pF tolerance capacitors were used in the design. The overall circuit size should be minimized as much as possible.

[3] The FET should be mounted as shown in the FP101 datasheet.